

FIG. 1

		Memory block							
		1	2	3	4	5	6	7	8
Time section	1	WF1							
	2		WF2						
	3			WF3					
	4				WF4				
	5					WB1			
	6						WB2		
	7	RF1				RB1		WB3	
	8								WB4
	9	WF1	RF2				RB2		
	10				WF2				
	11		WF3	RF3				RB3	
	12						WF4		
	13			WB1	RF4				RB4
	14						WB2		
	15	RF1		RB2	WB3				
	16								WB4
	17	WF1				RF2		RB2	
	18			WF2					
	19		RF3		RB3	WF3			
	20						WF4		
	21		WB1						
	22				WB2		RF4		RB4
	23	RF1	RB1				WB3		
	24								WB4
	1	WF1		RF2	RB2				
	2		WF2						
	3			WF3		RF3	RB3		
	4				WF4				
	5					WB1			
	6						WB2	RF4	RB4
	7	RF1				RB1		WB3	
	8								WB4

FIG. 3

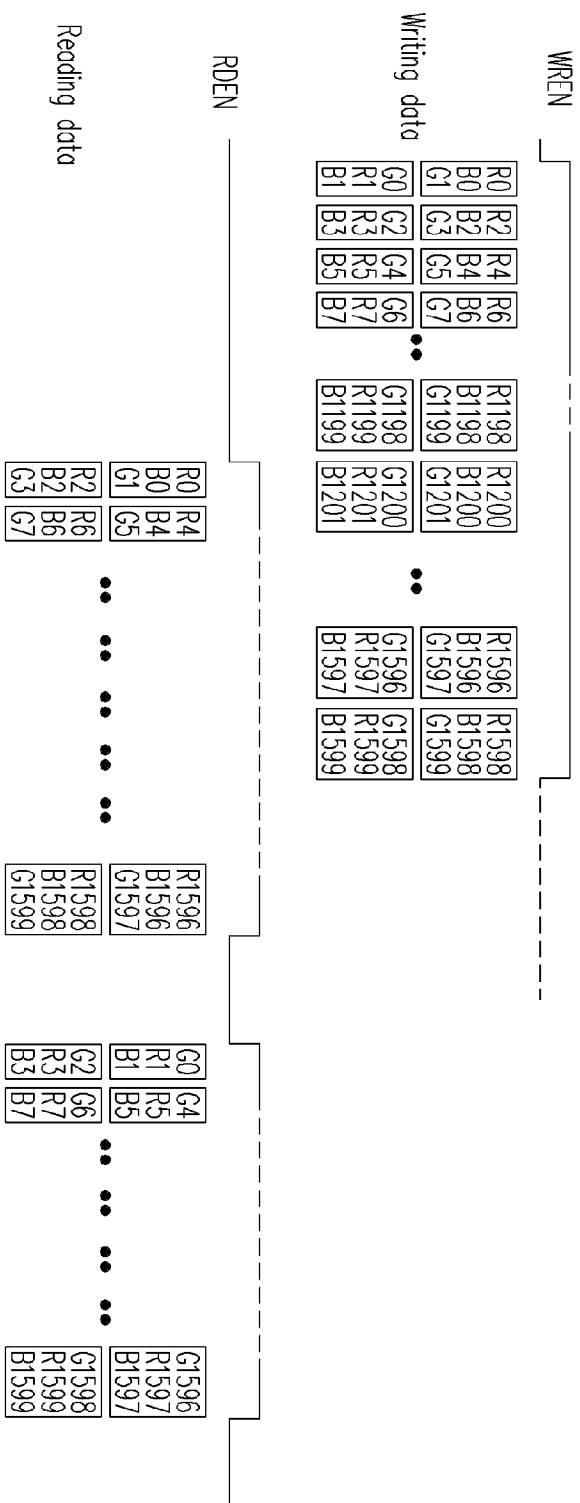


FIG. 4

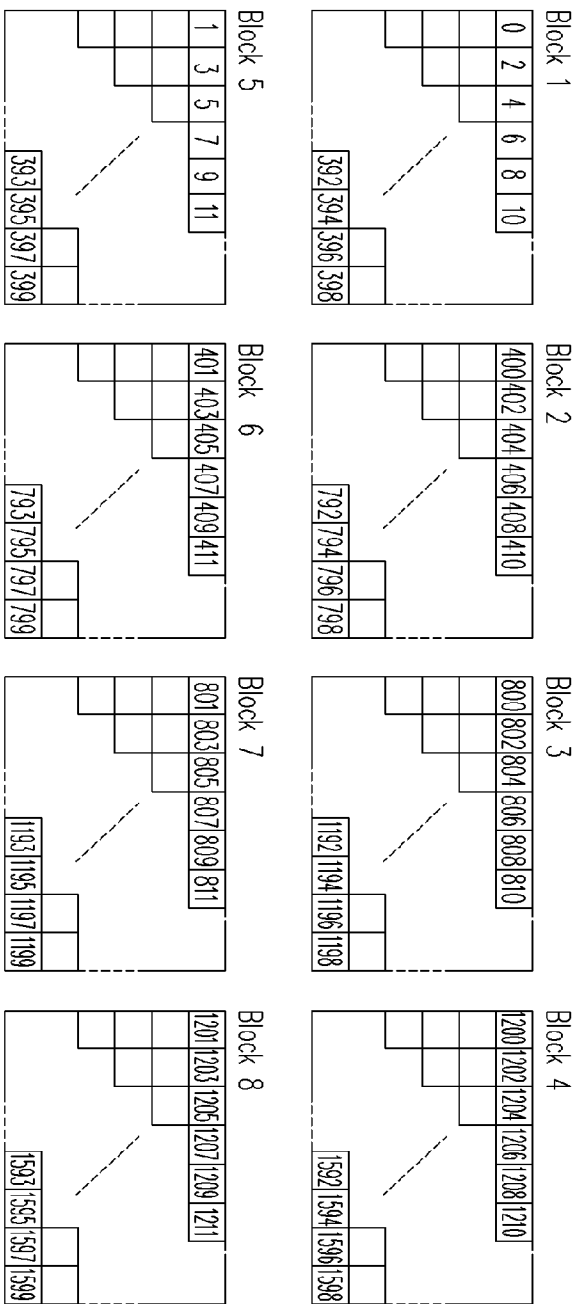


FIG. 5

		Memory block							
		1	2	3	4	5	6	7	8
Time section	1	WE1				W01			
	2								
	3		WE2				W02		
	4								
	5			WE3				W03	
	6								
	7	RE1			WE4				W04
	8		RE2						
	9	WE1	W01	RE3					
	10				RE4				
	11			WE2	W02	R01			
	12						R02		
	13					WE3	W03	R03	
	14								R04
	15	RE1						WE4	W04
	16			RE2					
	17	WE1		W01		RE3			
	18							RE4	
	19		R01			WE2		W02	
	20				R02				
	21		WE3		W03		R03		
	22								R04
	23	RE1					WE4		W04
	24					RE2			
	1	WE1	RE3			W01	RE4		
	2								
	3		WE2	R01			W02	R02	
	4								
	5			WE3	R03			W03	
	6								R04
	7				WE4				W04
	8								

FIG. 6